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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,063	03/11/2004	Howard Chih Hao Wang	2002-0276/2406.481	5688

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,063	WANG ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 12-14* is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 11* is/are allowed.

6)☒ Claim(s) *5,6,15 and 18-25* is/are rejected.

7)☒ Claim(s) *7-9,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II, claims 1-5 in the Paper filed 03/28/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 03/11/2004 is acceptable.

Drawings

3. The formal drawings filed on 03/11/2004 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 04/15/2004 has been considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21,23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by HASUNUMA (6,504,192).

Hasunuma discloses a transistor structure comprising (a) a semiconductor substrate 10 having isolation regions 11 and a plurality of transistor regions including first (B), second (C), and third (A) transistor regions comprised of a dielectric layer 1 formed on said substrate 10 between said isolation regions 11; (b) a gate electrode 2 having a first thickness formed on said dielectric layer 1 in said first (B) transistor region, a gate electrode 2 having a second thickness formed on said dielectric layer 1 in said second (C) transistor region, and a gate electrode 2 having a third thickness formed on said dielectric layer 1 in said third transistor region; (c) oxide spacers having a first width 3b formed adjacent to said gate electrode 2 in the first (B) transistor region, oxide spacers having a second width 3c that is less than said first width 3b formed adjacent to said gate electrode 2 in the second (C) transistor region, and oxide spacers having a third width 3a less than said second

width 3c formed adjacent to said gate electrode 2 in the third transistor region, 23. The transistor structure of claim 21 wherein said first thickness, said second thickness, and said third thickness are equivalent and the width of said oxide spacers is 10 to 500 nanometers (100-5000 Angstroms) and thus, for the most part, between about 10 and 1000 Angstroms. Note figure 5 and column 4 lines 51-67 of Hasunuma.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5,6,10,11,15,18-22,24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over PFIESTER (5,021,354) in view of AHN (5,874,330).

A. With regard to claims 5 and 6 the second (oxide only) embodiment of Pfiester discloses a method of forming multiple spacer structures comprising (a) providing a substrate 20-22 with isolation regions 80 and a plurality of transistor regions including first 22 and second 24 transistor regions comprised of a dielectric layer 24 on said substrate 20-22 between said isolation regions 80; (b) forming a first gate electrode 62 on said dielectric layer 24 in said first 22 transistor region and a second gate electrode 60 on said dielectric layer 24 in said second 20 transistor region; (c) forming an oxide layer 36-38 on the

substrate 20-22 and on the gate electrodes in said plurality of transistor regions; and (d) etching said oxide layer 36-38 to form spacers with a first width 66 adjacent to said first gate electrode 62, spacers having a second width 64 less than said first width 66 adjacent to said second gate electrode 60. Note figures 1-3, 8-10, column 3 lines 17-68, column 4 lines 1-41, and column 5 lines 29-68 of Pfiester. Pfiester discloses that one spacer width is appropriate for one type of channel, PMOS, and a second spacer width is appropriate for another type of channel, NMOS. There being only two types of channels, Pfiester discloses only two different spacer widths, not four different spacer widths as required by claim 6.

However, Ahn discloses a method of forming multiple spacer structures with different spacer widths for peripheral (logic) circuits than the spacer width appropriate for interior, memory circuits. Note the abstract, as well as column 1 lines 11-54 of Ahn. Therefore, it would have been obvious to a person having skill in the art to augment Pfiester's method of forming multiple spacer structures, by forming a first gate electrode with largest thickness in order to produce first spacers which, when etched, were wide enough to be appropriate for peripheral PMOS logic transistors, forming a second gate electrode with second largest thickness in order to produce second spacers which, when etched, were wide enough to be appropriate for peripheral NMOS logic transistors, forming a third gate electrode with smaller thickness in order to produce third spacers which, when etched, were wide enough to be appropriate for interior

memory PMOS logic transistors, and finally, forming a fourth gate electrode with smallest thickness in order to produce second spacers which, when etched, were wide enough to be appropriate for interior memory NMOS logic transistors, such as suggested by the combination of Pfeister's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer thicknesses, in order to form both CMOS transistors of both logic and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance.

B. With regard to claims 21,22,24, and 25 the second (oxide only) embodiment of Pfiester discloses a transistor structure comprising (a) a semiconductor substrate 20-22 having isolation regions 80 and a plurality of transistor regions including first 22 and second 24 transistor regions comprised of a dielectric layer 24 formed on said substrate 20-22 between said isolation regions 80; (b) a gate electrode having a first thickness formed on said dielectric layer 24 in said first 22 transistor region, a gate electrode having a second thickness formed on said dielectric layer 24 in said second 20 transistor region, and (c) oxide spacers having a first width 66 formed adjacent to said gate electrode in the first 22 transistor region and oxide spacers having a second width 64 that is less than said first width 66 formed adjacent to said gate electrode in the second 20 transistor region, wherein said first thickness is greater than said second thickness and the width of said oxide spacers is 20 nanometers (200 Angstroms), which is between about 10 and 1000

Angstroms. Note figures 1-3, 8-10, column 3 lines 17-68, column 4 lines 1-41, and column 5 lines 29-68 of Pfiester. Pfiester discloses that one spacer width is appropriate for one type of channel, PMOS, and a second spacer width is appropriate for another type of channel, NMOS. There being only two types of channels, Pfiester discloses only two different spacer widths, not three different spacer widths as required by claims 22 and 24, or four different spacer widths as required by claim 25.

However, Ahn discloses a transistor structure with different spacer widths for peripheral (logic) circuits than the spacer widths appropriate for interior, memory circuits. Note the abstract, as well as column 1 lines 11-54 of Ahn. Therefore, it would have been obvious to a person having skill in the art to augment Pfiester's transistor structure by forming a first gate electrode with largest thickness in order to produce first spacers which, when etched, were wide enough to be appropriate for peripheral PMOS logic transistors, forming a second gate electrode with second largest thickness in order to produce second spacers which, when etched, were wide enough to be appropriate for peripheral NMOS logic transistors, forming a third gate electrode with smaller thickness in order to produce third spacers which, when etched, were wide enough to be appropriate for interior memory PMOS logic transistors, and finally, forming a fourth gate electrode with smallest thickness in order to produce fourth spacers which, when etched, were wide enough to be appropriate for interior memory NMOS logic transistors, such as suggested by the combination of Pfeister's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer

thicknesses, in order to form both CMOS transistors of both logic and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance.

C. With regard to claims 15 and 18-20 the first (nitride and oxide) embodiment of Pfiester discloses a transistor structure comprising (a) a semiconductor substrate 20-22 having isolation regions 80 and a plurality of transistor regions including first 20 and second 22 transistor regions comprised of a dielectric layer 24 formed on said substrate 20-22 between said isolation regions 80; (b) a gate electrode 40-44 having a first thickness formed on said dielectric layer 24 in said first 20 transistor region, a gate electrode 42-46 having a second thickness formed on said dielectric layer 24 in said second 22 transistor region, and (c) oxide spacers having a width formed adjacent to said gate electrodes in said first and second transistor regions; and (d) silicon nitride spacers 54 having a first width formed on said oxide spacers in said first 20 transistor region, and silicon nitride spacers 56 having a second width less than said first width 54 formed on said oxide spacers in said second 22 transistor region, 18. The transistor structure of claim 15 wherein the width of said oxide spacers is 20 nm (200 Angstroms), which is between about 10 and 1000 Angstroms, and the first and second widths of said silicon nitride spacers are 100-350 nanometers, which includes the interval between about 10 and 1000 Angstroms. Note figures 1-7, 10, column 3 lines 17-68, column 4 lines 1-68, and column 5 lines 1-28 of Pfiester. Pfiester discloses that one spacer width is appropriate for one type of channel, PMOS, and a second spacer width is appropriate

for another type of channel, NMOS. There being only two types of channels, Pfiester discloses only two different spacer widths, not three different spacer widths as required by claims 18 and 19, or four different spacer widths as required by claim 20.

However, Ahn discloses a transistor structure with different spacer widths for peripheral (logic) circuits than the spacer widths appropriate for interior, memory circuits. Note the abstract, as well as column 1 lines 11-54 of Ahn. Therefore, it would have been obvious to a person having skill in the art to augment Pfiester's transistor structure by forming a first gate electrode with largest thickness in order to produce first spacers which, when etched, were wide enough to be appropriate for peripheral PMOS logic transistors, forming a second gate electrode with second largest thickness in order to produce second spacers which, when etched, were wide enough to be appropriate for peripheral NMOS logic transistors, forming a third gate electrode with smaller thickness in order to produce third spacers which, when etched, were wide enough to be appropriate for interior memory PMOS logic transistors, and finally, forming a fourth gate electrode with smallest thickness in order to produce fourth spacers which, when etched, were wide enough to be appropriate for interior memory NMOS logic transistors, such as suggested by the combination of Pfeister's teaching concerning PMOS vs. NMOS spacer thickness with Ahn's teaching concerning peripheral vs. interior spacer thicknesses, in order to form both CMOS transistors of both logic and memory types on a single chip to thus provide a memory chip with peripheral logic, both the memory and logic having optimal performance.

Allowable Subject Matter

8. Claims 10 and 11 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a method of forming multiple spacer widths on a substrate, comprising the steps of (a) providing a substrate with isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer on said substrate between said isolation regions; (b) forming a first gate electrode on said dielectric layer in said first transistor region, a second gate electrode on said dielectric layer in said second transistor region, and a third gate electrode on said dielectric layer in said third transistor region, said first gate electrode having a thickness equal to the thickness of said second gate electrode and said third gate electrode having a thickness less than the thickness of said first and second gate electrodes; (c) forming an oxide layer on said substrate in the plurality of transistor regions; (d) forming a first silicon nitride layer on said oxide layer in said first transistor region; (e) forming a second silicon nitride layer on said first silicon nitride layer in said first transistor region and on said oxide layer in said second and third transistor regions; and (f) etching through said silicon nitride layers and through said oxide layer to form spacers having a first width adjacent to said first electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers

having a third width less than said second width adjacent to said third gate electrode, as recited in claim 10. Note that the method of claim 10 makes the device of claim 17, including the feature that two gate electrodes, bounded by silicon nitride spacers of different widths, have the same thickness, while a third gate electrode, bounded by a silicon nitride spacer of a smaller width, be of a smaller thickness. In view of Pfeister's discovery that thin gate electrodes tend to have narrower spacers, it is counterintuitive to find two gate electrodes of the same thickness having spacers of different widths.

9. Claims 7-9,16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

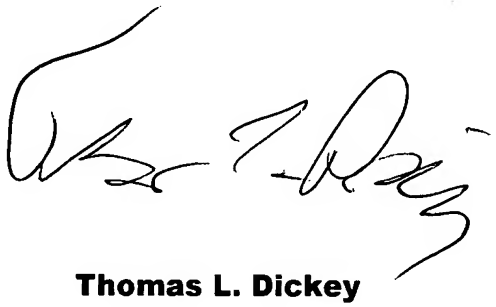
Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/05